AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph within the clean version of the substitute specification beginning at page 2, line 18, with the following rewritten paragraph.

-- However, the above-mentioned configuration always lets signals pass the ΔΣ modulator 93. Even if no volume adjustment or the like is needed, namely, the factor k is 1.0, music data D11 ~~D1i~~ always passes the ΔΣ modulator 93, degrading sound quality. A fraction eliminator 94 is used for performing specified addition and subtraction to eliminate a fraction remaining in an integrator inside the ΔΣ modulator 93. This operation approximates patterns for an original sound signal D11 ~~D1i~~ and a ΔΣ modulation signal D1'. A delay circuit 96 is used to approximately align phases for the ΔΣ modulation signal D1' and the original sound signal D1i. A control unit 97 monitors signal patterns for the ΔΣ modulation signal D1' and the original sound signal D11 ~~D1i~~. When these patterns almost match, a selector 95 is switched to side a for the delayed original sound signal D1d from side b for the ΔΣ modulation signal D1'. --

Please replace the paragraph within the clean version of the substitute specification beginning at page 3, line 3, with the following rewritten paragraph.

-- When no volume adjustment or the like is needed, this process can switch the ΔΣ modulation signal D1' over to the delayed original sound signal D11 ~~D1i~~ and generate a 1-bit data output from an output terminal 95 without generating a switching noise or the like. This process also can bypass reprocessing in the ΔΣ modulator 93. --

Please replace the paragraph within the clean version of the substitute specification beginning at page 3, line 8, with the following rewritten paragraph.

-- However, ~~a~~ noise may be generated during this switching operation, depending on the specifications of the ΔΣ modulator 93 to be used and the frequency of the 1-bit data D11 ~~D1i~~ to be input. Generally, a high-order ΔΣ modulator can provide a high S/N ratio in an audible

band. On the other hand, frequency characteristics change at a point near the audible band. A phase can easily rotate at a high frequency. When high-order ΔΣ modulation is used and the input signal frequency is high, a level difference and a phase shift occurs between the delayed original sound signal D11 ~~Di~~ and the ΔΣ modulation signal D1'. ~~A noise~~ Noise occurs when the selector 95 switches between these signals. --

Please replace the paragraph within the clean version of the substitute specification beginning at page 3, line 19, with the following rewritten paragraph.

-- When the low-order ΔΣ modulator 93 is used, it hardly generates a noise during switchover because of little level difference and phase rotation. On the other hand, the audible band causes a low S/N ratio, lowering the S/N ratio ~~ration~~ when the ΔΣ modulator 93 is not bypassed. --

Please replace the paragraph within the clean version of the substitute specification beginning at page 5, line 10, with the following rewritten paragraph.

-- Embodiments of the present invention will be described in further detail with reference to the accompanying drawings. As shown in FIG. 3, this embodiment is a 1-bit data editing unit 10 which applies edit processing including fading such as fade-in and fade-out to music data D11 ~~Di~~ comprising 1-bit data resulting from ΔΣ modulation. --

Please replace the paragraph within the clean version of the substitute specification beginning at page 5, line 16, with the following rewritten paragraph.

-- The 1-bit data editing unit 10 comprises a multiplier 12, a ΔΣ modulator 13, a delay circuit 17, a selector 16, and a control unit 18. The multiplier 12 multiplies input 1-bit data D11 ~~Di~~ by a factor k. The input 1-bit data D11 ~~Di~~ is the above-mentioned music data to

be input to an input terminal 11. The ΔΣ modulator 13 comprises, e.g, five integrators and reapplies ΔΣ modulation to a multiplied output from the multiplier 12 by varying effective orders, as will be described later. The delay circuit 17 aligns a phase for the input 1-bit data D11 ~~D1i~~ to the reprocessed ΔΣ modulation signal D1' from the ΔΣ modulator 13. The selector 16 switches between the delayed original sound signal D1d output from the delay circuit 17 and the reprocessed ΔΣ modulation signal D11 ~~D1i~~. The control unit 18 provides controls to vary the effective orders for the ΔΣ modulator 13. --

Please replace the paragraph within the clean version of the substitute specification beginning at page 10, line 27, with the following rewritten paragraph.

-- The following describes the operations of the 1-bit data editing unit 10 in detail with reference back to FIG. 3. In FIG. 3, like the prior art, a 1-bit data D11 ~~D1i~~ is input to the input terminal 11 as an original sound signal. The multiplier 12 multiplies the input 1-bit data D11 ~~D1i~~ by a factor k (any value) to generate a multi-bit multiplication output with an adjusted sound volume. The ΔΣ modulator 13 receives this output and converts it to 1-bit data to generate the ΔΣ modulation signal D1'. --

Please replace the paragraph within the clean version of the substitute specification beginning at page 11, line 24, with the following rewritten paragraph.

-- When the fraction has been removed, the control unit 18 compares the ΔΣ modulation signal D1' with the delayed original sound signal D11 ~~D1i~~. When the output patterns match within an appropriate range, the control unit 18 switches the selector 16 over to the delayed original sound signal D11 ~~D1i~~ side a. --